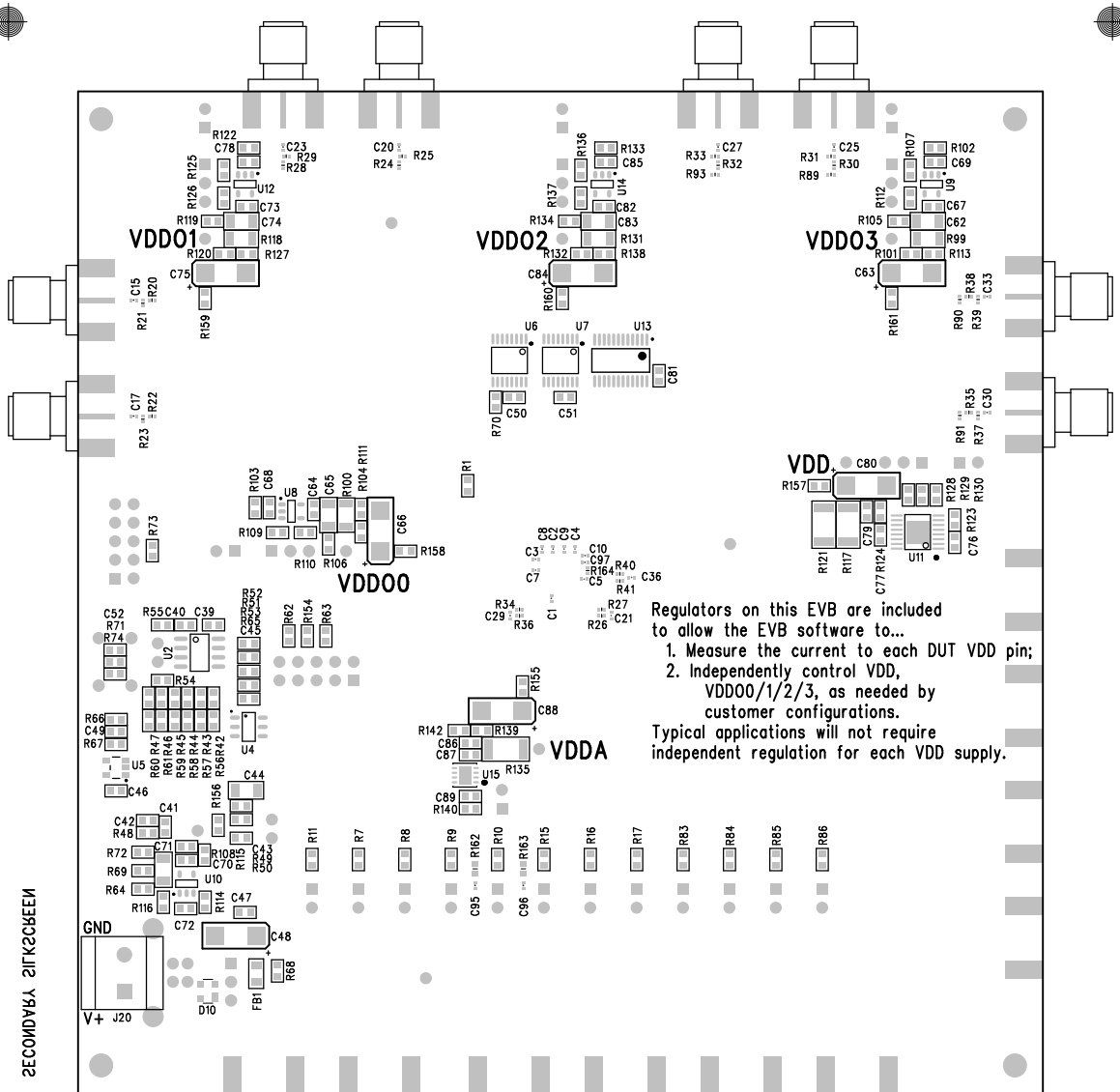
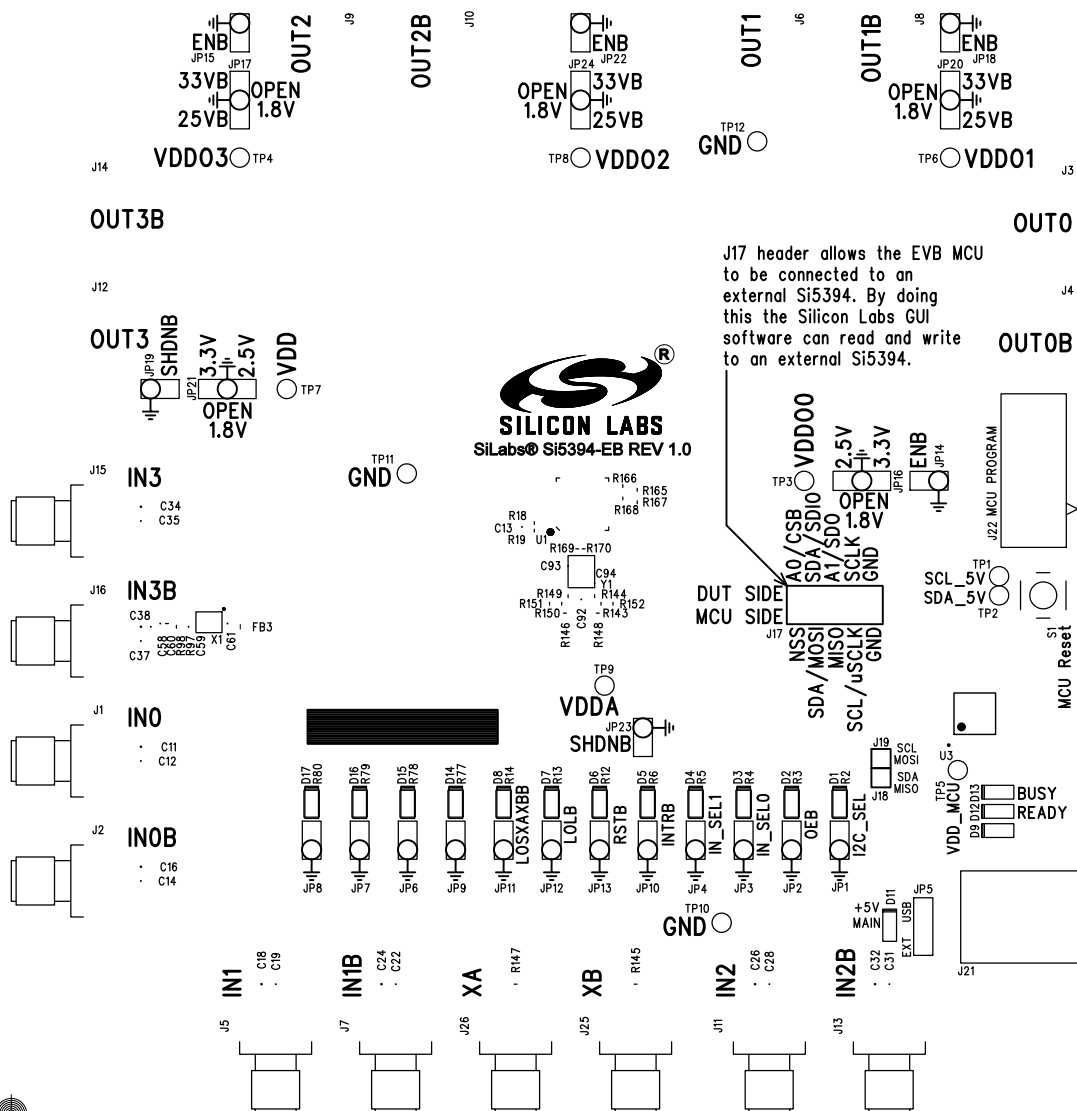


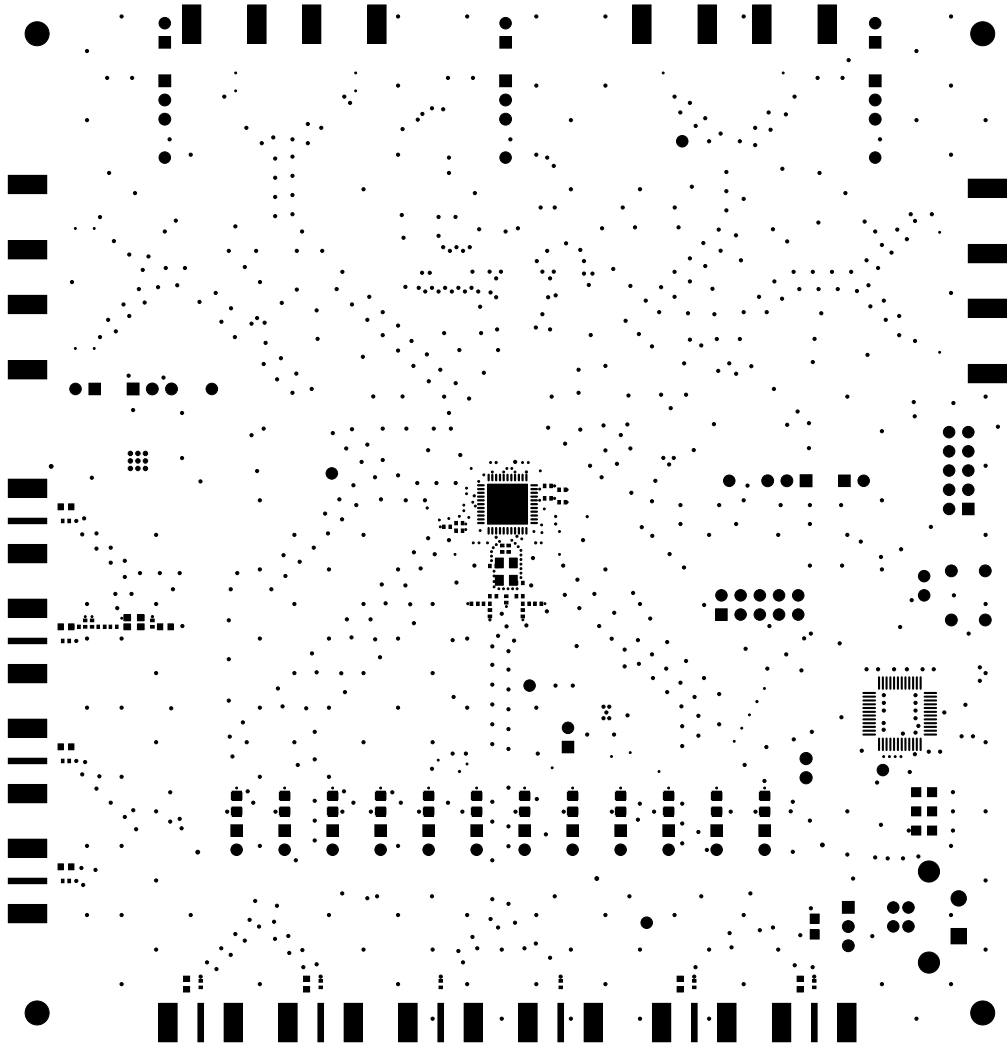


Regulators on this EVB are included to allow the EVB software to...

1. Measure the current to each DUT VDD pin;
2. Independently control VDD, VDD00/1/2/3, as needed by customer configurations.

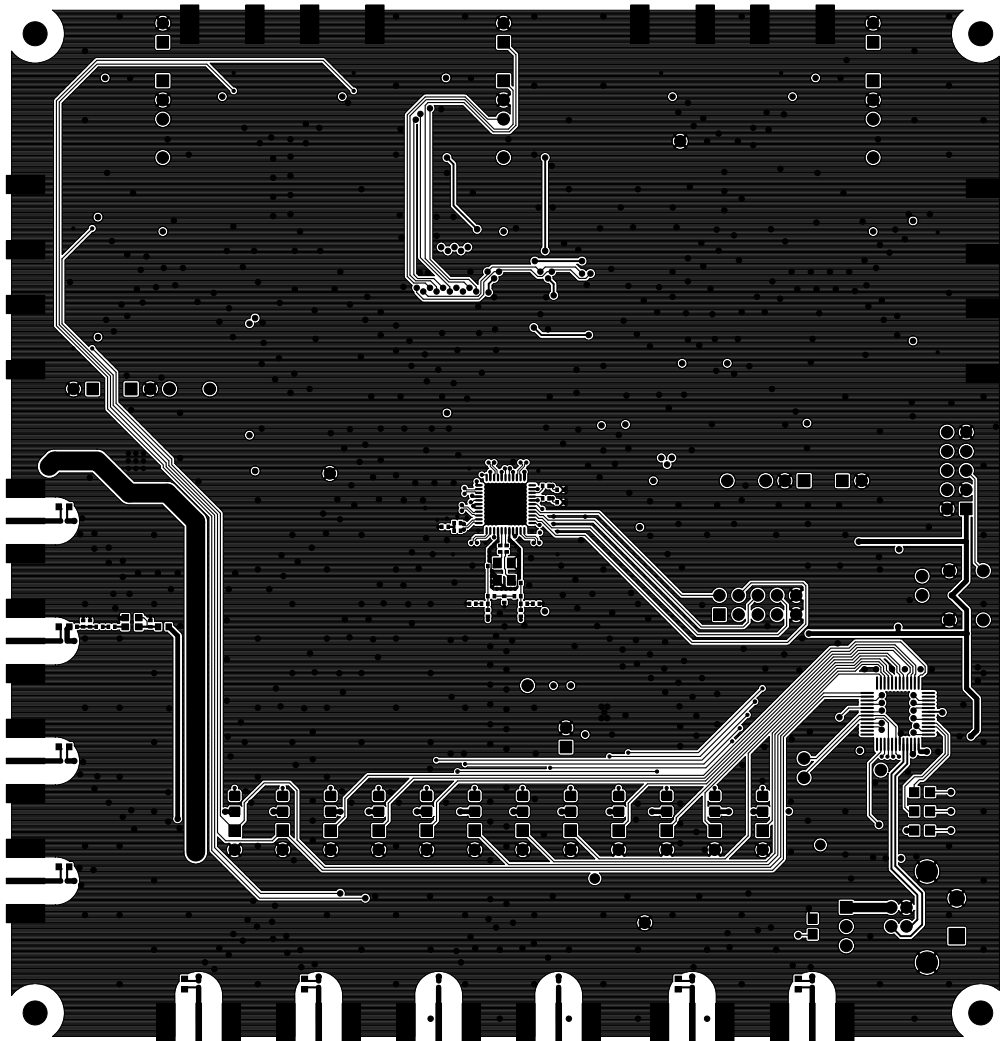
Typical applications will not require independent regulation for each VDD supply.



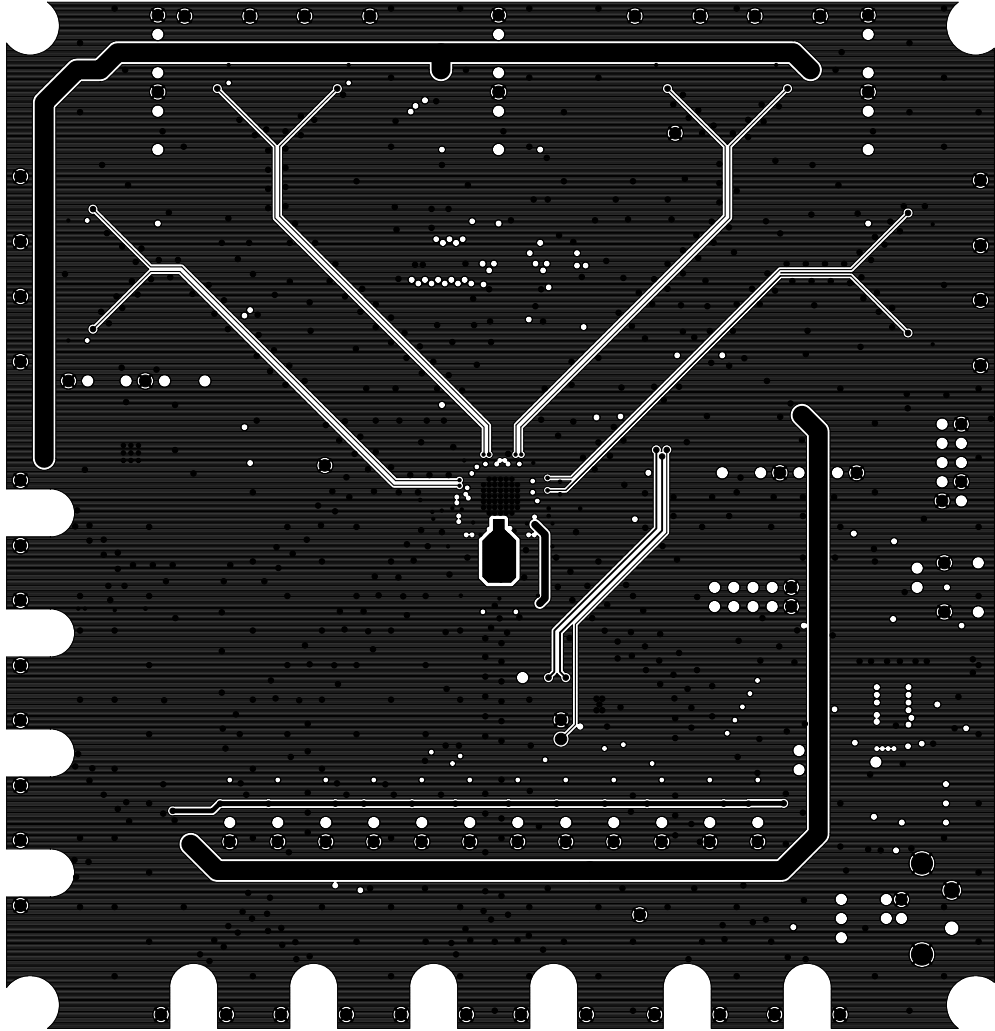


PRIMARY SOLDER MASK



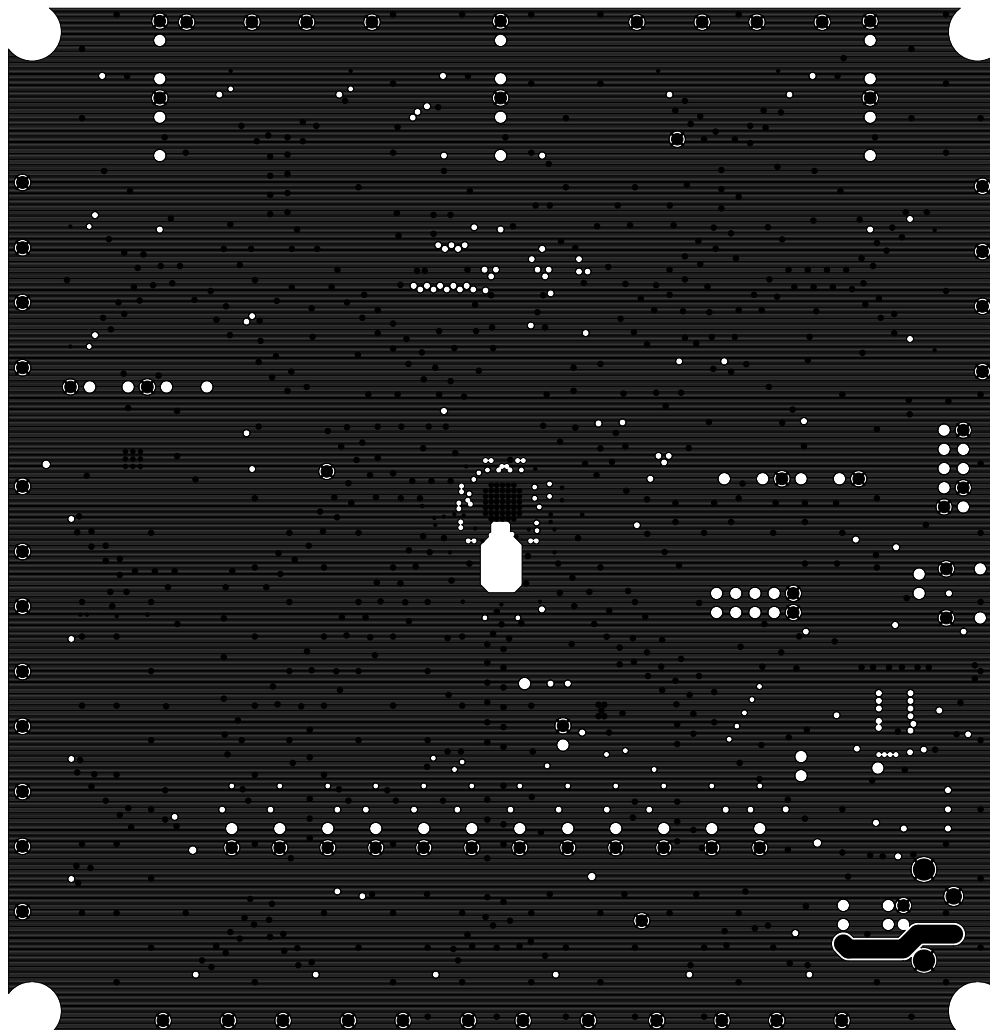


PRIMARY SIDE



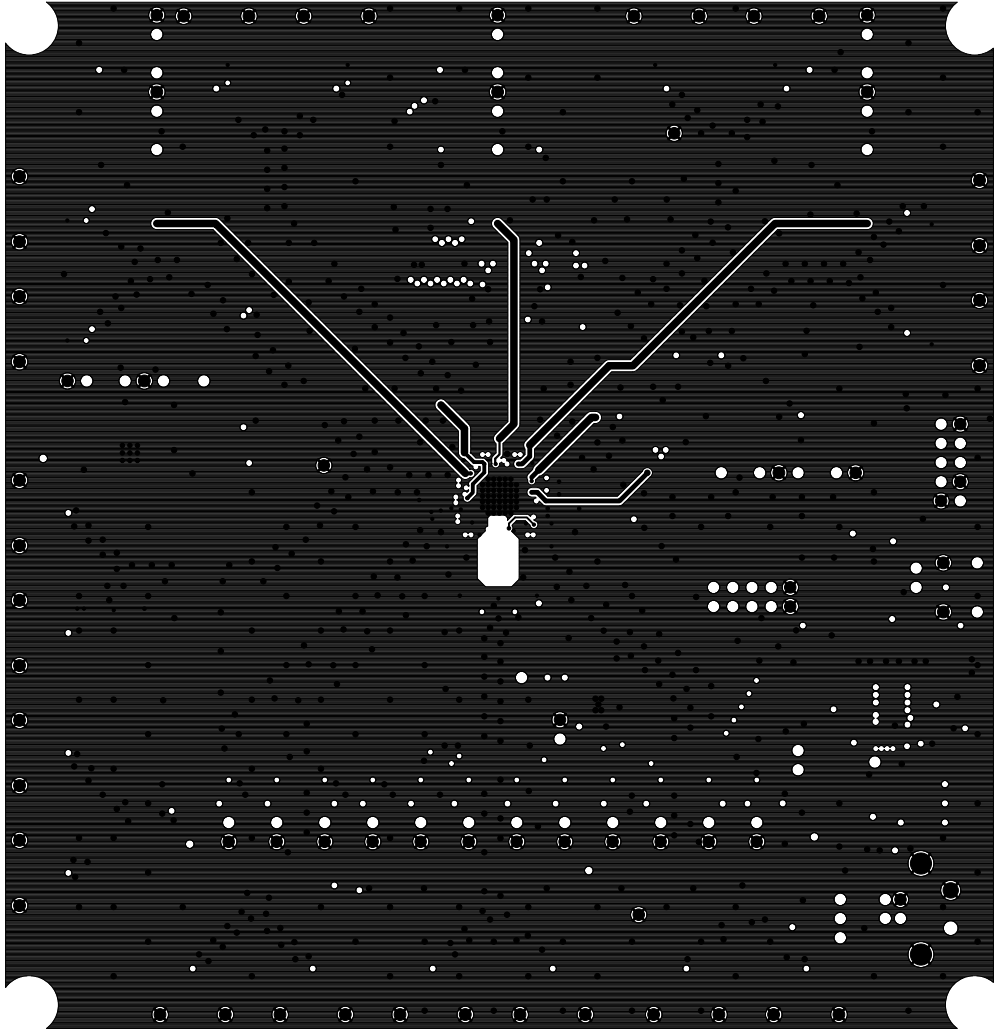
L02





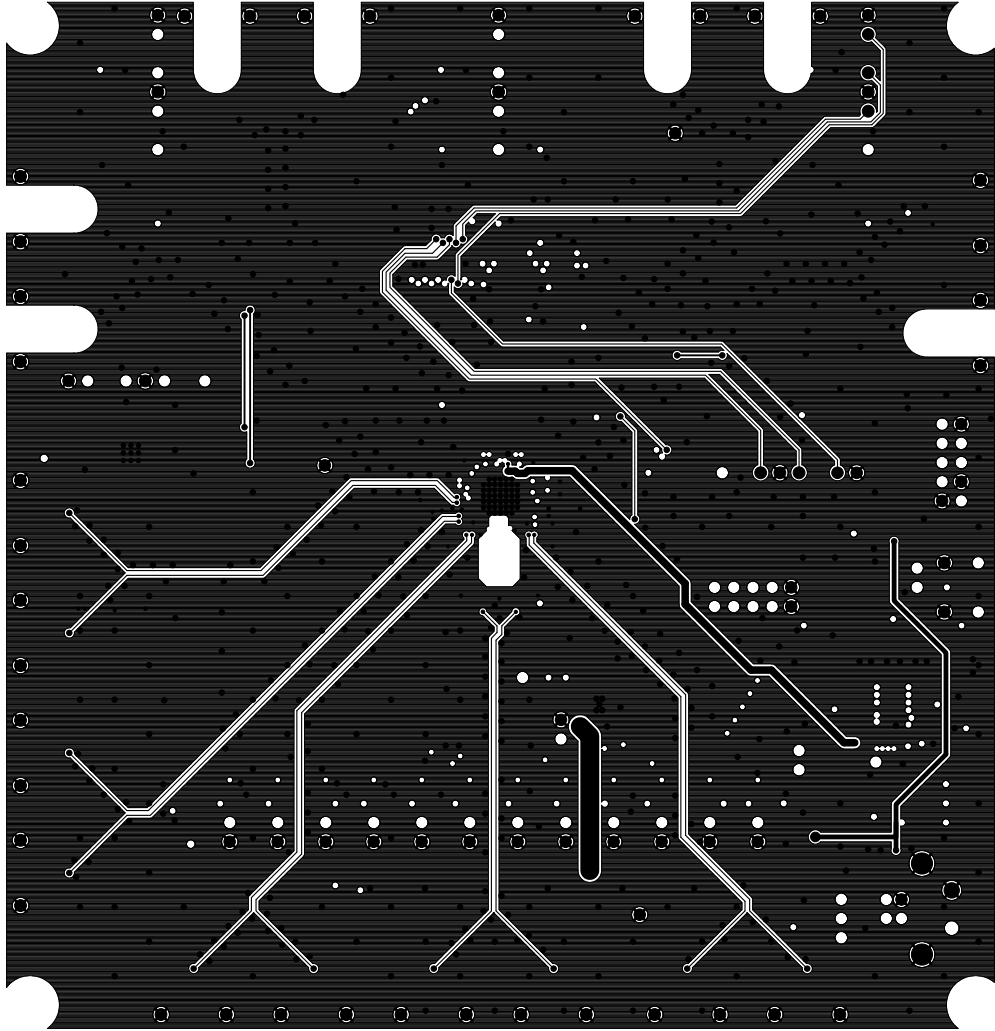
L03





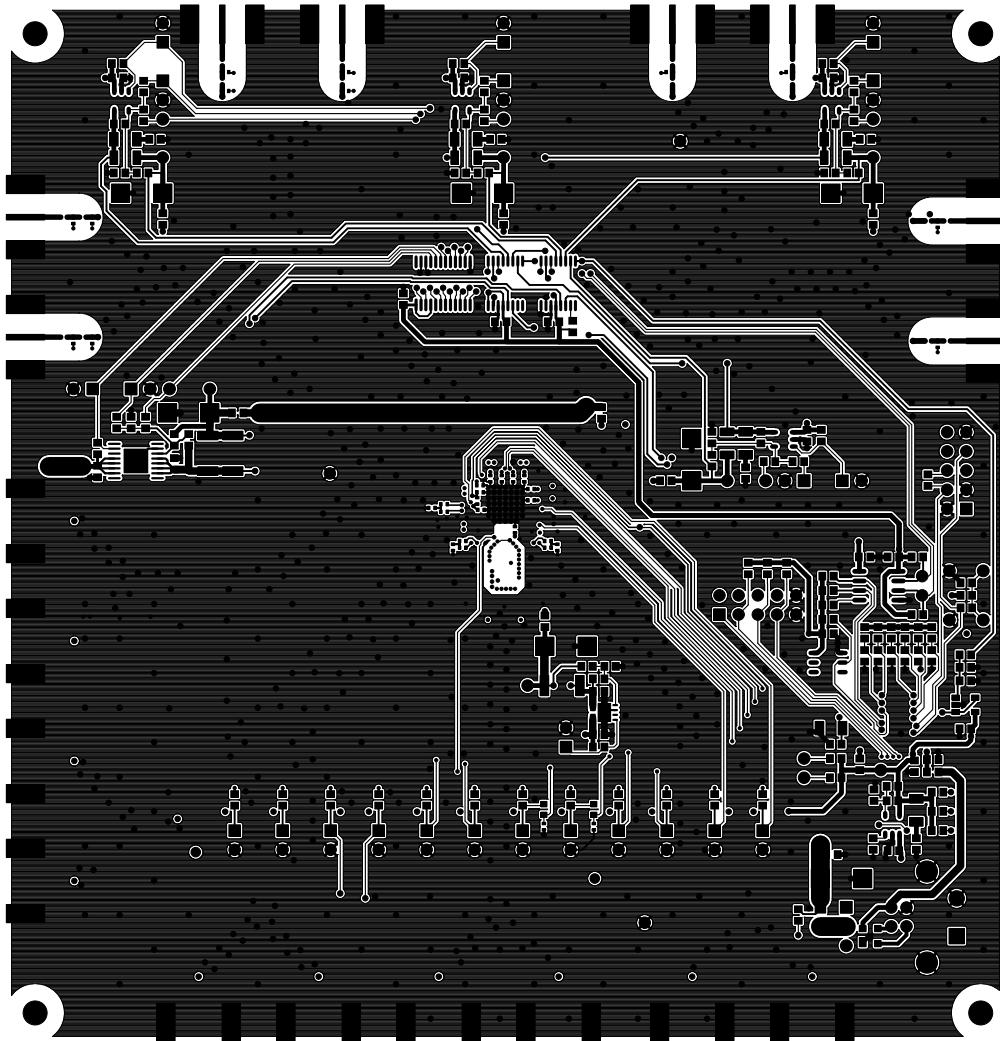
L04



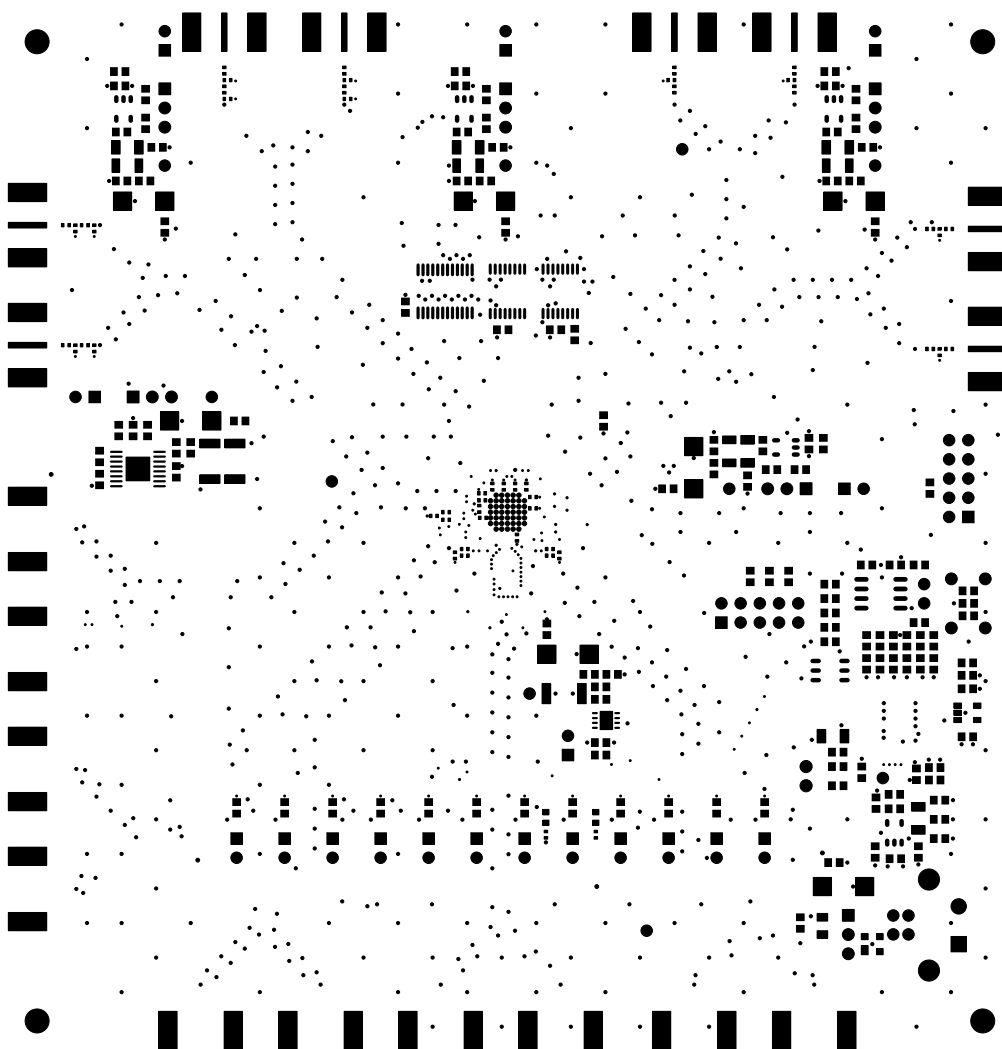


L05





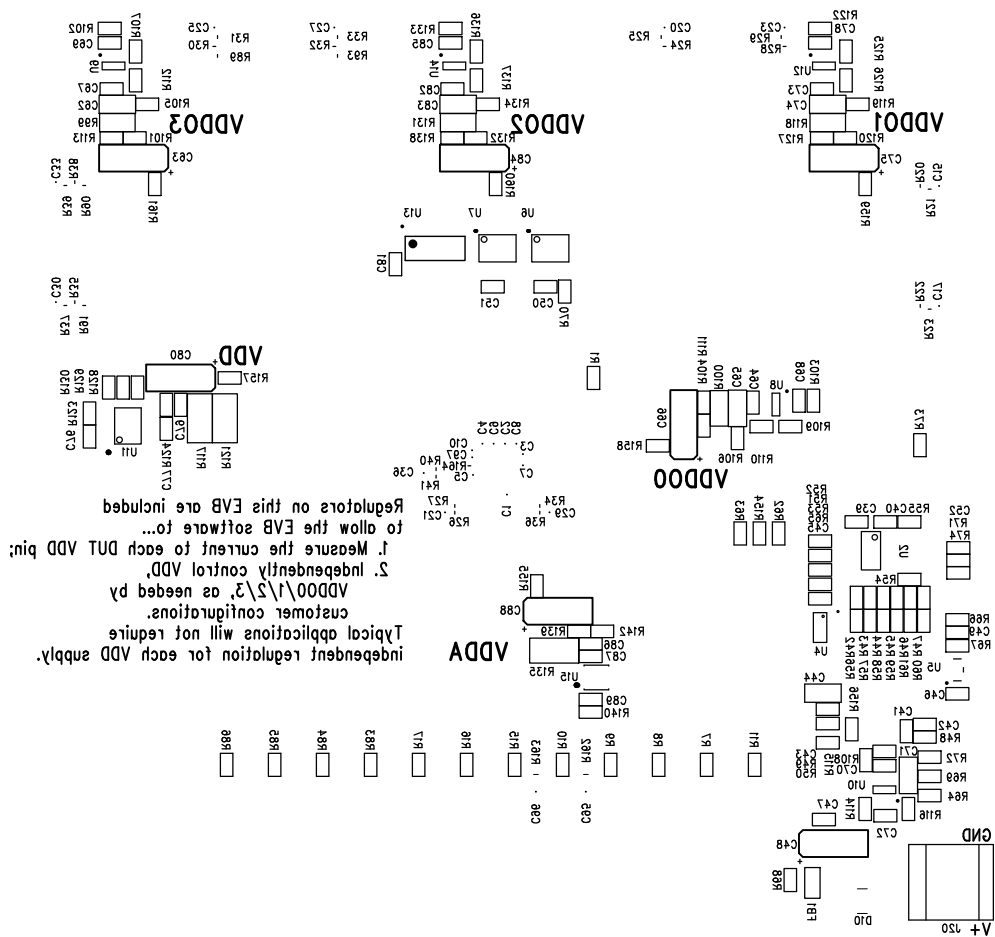
SECONDARY SIDE

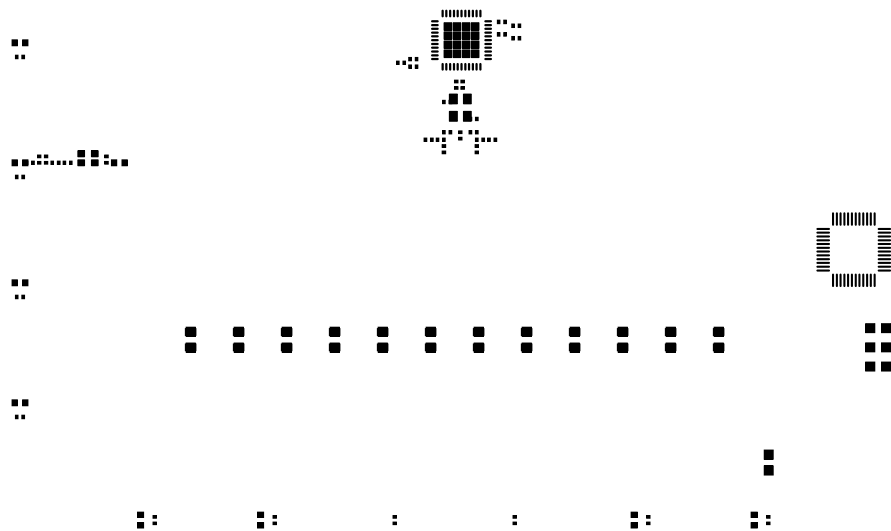


SECONDARY SOLDER MASK



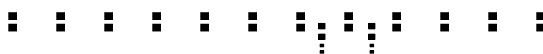
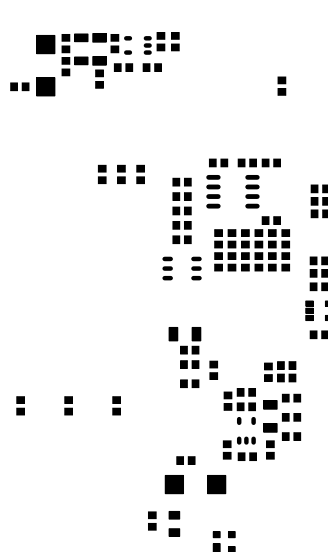
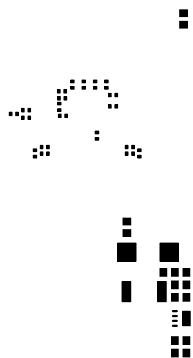
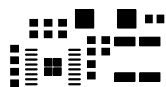
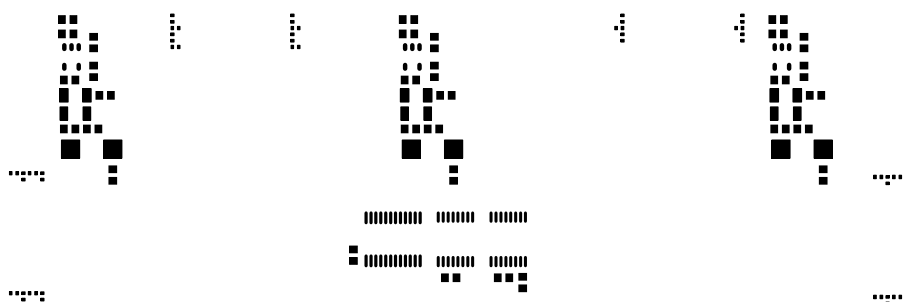
SECONDARY SILKSCREEN





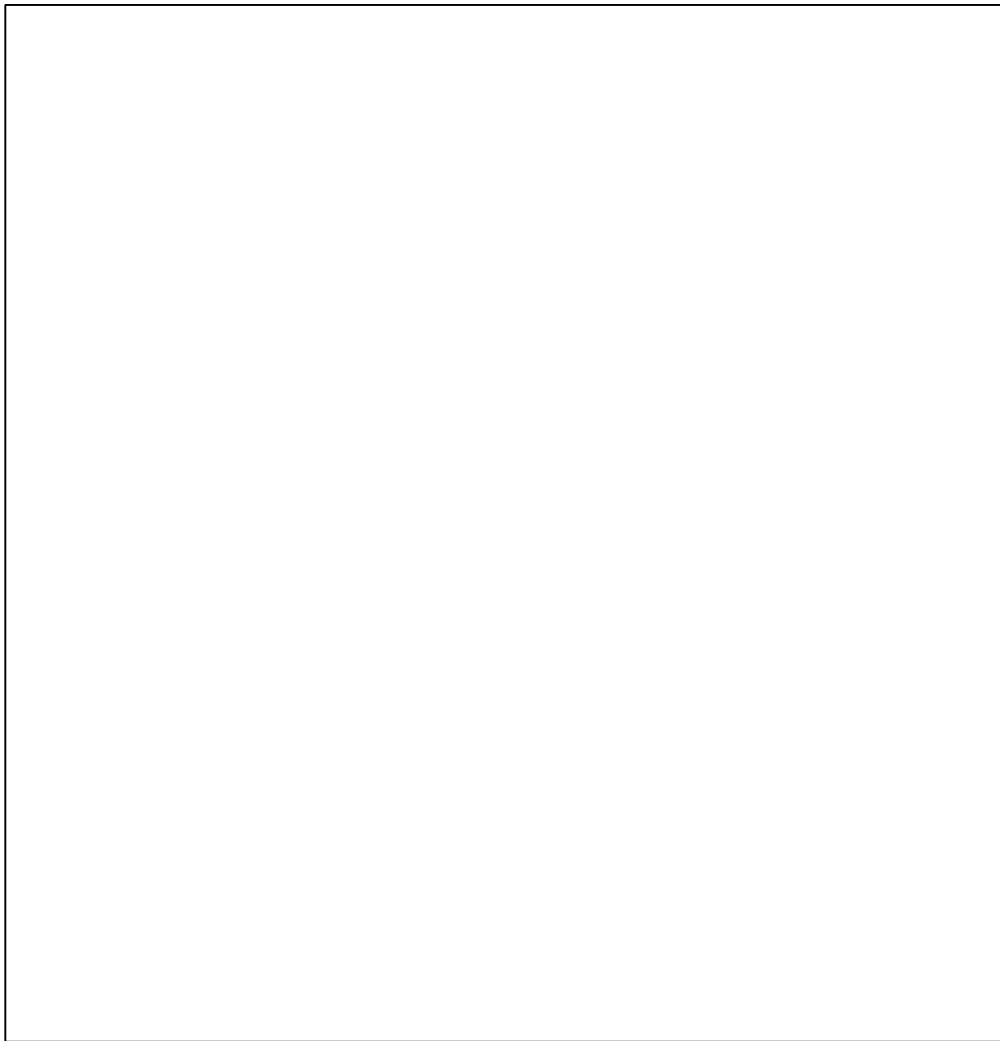
PRIMARY SOLDER PASTE

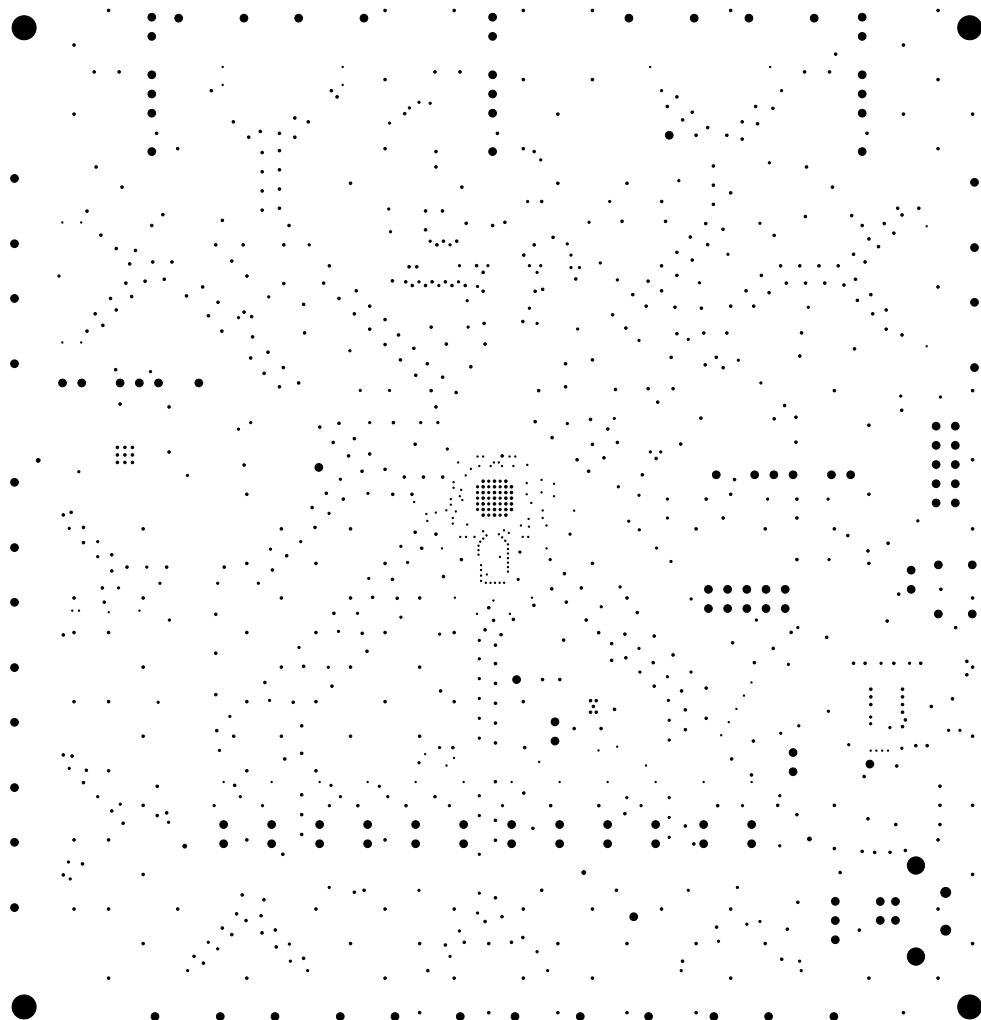


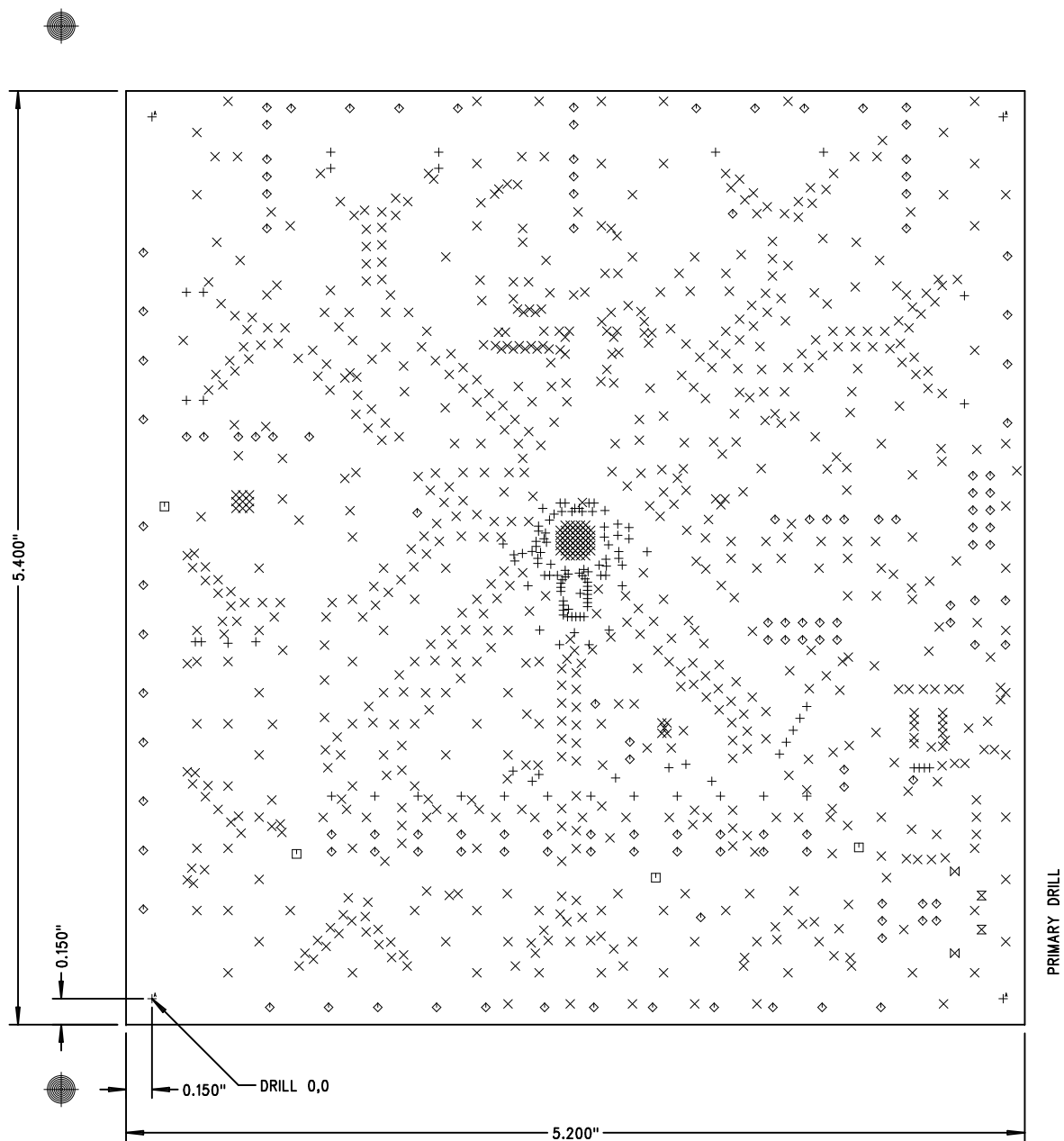


SECONDARY SOLDER PASTE









- NOTES : UNLESS OTHERWISE SPECIFIED
1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
 2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
 3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE $\geq 345^{\circ}\text{C}$, COLOR, NATURAL.
 4. COPPER WEIGHT SHALL BE 0.5 OZ./SQ. FT. BEFORE PLATING.
 5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
 6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE $\pm 0.003"$.
 7. MINIMUM ANNULAR RING SHALL BE 0.001".
 8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
 9. FINAL PCB THICKNESS SHALL BE 0.062" $\pm 10\%$.
 10. WARP/TWIST SHALL NOT EXCEED 1.0%.
 11. FINISH SHALL BE LPI, BLUE SMOBC, ENIG BOTH SIDES.
 12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
 13. INTERNAL 0.157MM TRACES TO BE 50 OHM $Z_0 \pm 5\%$.
TOP 0.725MM TRACES TO BE 50 OHM $Z_0 \pm 5\%$ REF TO L03.
BOTTOM 0.725MM TRACES TO BE 50 OHM $Z_0 \pm 5\%$ REF TO L04.
 14. VENDOR TO PROVIDE PCB MICRO-SECTION OF COUPON AREA & TDR TEST REPORT.
 15. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT

LAYER STACKUP	FILE NAMES
PRIMARY SILKSCREEN	53xx-EB44_PSS.PHO
PRIMARY SOLDERMASK	53xx-EB44_PSM.PHO
PRIMARY SIDE	53xx-EB44_PRI.PHO
• 370HR - 7MIL THK	
RF ROUTE/GND	53xx-EB44_L02.PHO
• 370HR - 7MIL THK	
GROUND PLANE	53xx-EB44_L03.PHO
370HR	
POWER ROUTE/GND	53xx-EB44_L04.PHO
• 370HR - 7MIL THK	
RF ROUTE/GND	53xx-EB44_L05.PHO
• 370HR - 7MIL THK	
SECONDARY SIDE	53xx-EB44_SEC.PHO
SECONDARY SOLDERMASK	53xx-EB44_SSM.PHO
SECONDARY SILKSCREEN	53xx-EB44_SSS.PHO

SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TOL
0.007	130	+	P	1	+0/-0.007
0.013	828	×	P	2	+0/-0.013
0.020	4	□	P	3	+/-0.003
0.040	132	◇	P	4	+/-0.003
0.052	2	⊗	P	5	+/-0.003
0.091	2	⊠	P	6	+/-0.003
0.125	4	A	N	7	+/-0.003

UNLESS OTHERWISE SPECIFIED			THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF SILICON LABORATORIES, INC.			COMPANY:  400 W CESAR CHAVEZ ST. AUSTIN, TX 78701 (512)416-8500 www.silabs.com					
DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH DIMENSIONS IN BRACKETS [] ARE IN MILLIMETERS INTERPRET DRAWING PER MIL-D-1000						NAME: Si53xx-EB44			REV : 1.0		
TOLERANCES											
HOLE TOLERANCES PER 78027											
DECIMALS .XX +/- .XXX +/-	ANGLES +/-	SURFACES MICROINCHES	DESIGN	TT	27NOV2017	SIZE B	PART NUMBER:				
PART TO BE FREE OF BURRS			LAYOUT	CT	30NOV2017						
BREAK EDGES MAX	BEND RADIUS MAX	BEND RELIEF MAX	DO NOT SCALE DRAWING			SCALE 1:1		FABRICATION DRAWING			
						SHEET 1 OF 1					